

I claim:

1. A frequency synthesizer for producing an output signal with an output frequency higher than an input frequency, the synthesizer comprising:

5 a plurality of phase signals having a reference frequency;

10 - a multiplexer coupled to receive the plurality of phase signals, the multiplexer having a multiplexer output signal based on at least one of the plurality of phase signals; and

15 - a phase selector coupled to receive the multiplexer output signal, the phase selector having a selector output which selects the multiplexer output signal;

20 wherein

25 - each phase signal is out of phase with the other phase signal by a multiple of a predetermined time interval,

30 - the selector output is received by the multiplexer and

35 the multiplexer output is the output signal.

40 2. A frequency synthesizer as in claim 1 wherein the multiplexer output is chosen from the plurality of phase signals and a new phase signal is chosen as the multiplexer output by the phase selector 5 on the occurrence of either a rising edge of the multiplexer output or a falling edge of the multiplexer output.

3. A frequency synthesizer as in claim 2  
wherein each successive phase signal chosen by the phase  
selector leads ~~its~~ predecessor by a multiple of the  
predetermined time interval.

4. A frequency synthesizer as in claim 3  
wherein the multiphase reference generator is a phase  
generator coupled to receive a reference signal having  
the reference frequency and wherein the plurality of  
phase signals is based on the reference signal.

5 (b) 5. A frequency synthesizer as in claim 4  
wherein the phase generator is chosen from the group  
comprising:

a ring oscillator;  
a Johnson counter circuit; and  
a delay locked loop circuit.

6. A frequency synthesizer as in claim 5  
wherein the multiplexer selects one out of a plurality  
of <sup>possible</sup> phase signals from the phase generator as  
the multiplexer output based on a select word.

7. A frequency synthesizer as in claim 6  
wherein the phase selector is a binary digital  
accumulator clocked by the multiplexer output.

8. A frequency synthesizer as in claim 7  
wherein the binary digital accumulator adds a  
predetermined binary control word to a binary stored  
value on each cycle of the multiplexer output, and  
wherein selected bits of the binary stored value forms  
the selector output.

9. A frequency synthesizer as in claim 8  
wherein the selector output is transmitted to the  
multiplexer as the select word.

10. A frequency synthesizer as in claim 1  
wherein the multiplexer output is produced from at least  
two phase signals chosen from the plurality of phase  
signals.

11. A frequency synthesizer as in claim 10  
wherein each successive multiplexer output determined by  
the selector output leads its predecessor by a multiple  
of the predetermined time interval.

12. A frequency synthesizer as in claim 11  
wherein the multiphase reference generator is a phase  
generator coupled to receive a reference signal having  
the reference frequency and wherein the plurality of  
phase signals is based on the reference signal.

13. A frequency synthesizer as in claim 12  
wherein the phase generator is chosen from the group  
comprising:

5 a ring oscillator;  
a Johnson counter circuit; and  
a delay locked loop circuit.

14. A frequency synthesizer as in claim 11  
wherein the multiplexer comprises:

5 a multiplexer circuit which selects at least  
two selected phase signals out of the plurality of phase  
signals; and

10                   a signal blender/interpolator coupled to receive the selected phase signals from the multiplexer, the signal blender/interpolator producing the multiplexer output; and

10                   wherein

15                   the signal blender/interpolator blends the selected phase signals to produce the multiplexer output, and

15                   at least two selected phase signals are selected based on a portion of a select word.

15. A frequency synthesizer as in claim 14 wherein the multiplexer output includes a variable delay determined by a delay between the selected phase signals and a first portion of the select word.

16. A frequency synthesizer as in claim 14 wherein the phase selector is a binary digital accumulator clocked by the multiplexer output.

17. A frequency synthesizer as in claim 16 wherein the binary digital accumulator adds a predetermined binary control word to a binary stored value on each cycle of the multiplexer output, and wherein selected bits of the binary stored value forms the selector output.

18. A frequency synthesizer as in claim 17 wherein the selector output is transmitted to the multiplexer means as the select word.

19. A frequency synthesizer comprising:

5                   - a phase generator coupled to receive an input signal having a reference frequency and generating a plurality of phase signals having a frequency substantially equal to a reference frequency, each phase signal being out of phase with the input signal by a multiple of a predetermined time interval,

10                  - a multiplexer means coupled to receive the plurality of phase signals and producing a multiplexer output,

15                  - a phase selector clocked by the multiplexer output and producing a selector output transmitted to the multiplexer means and

20                  - a predetermined control word transmitted to the phase selector, the control word being added by the phase selector to a stored value on every cycle of the multiplexer output

25                  wherein

30                  - the multiplexer output is selected by the selector output and is based on at least one of the plurality of phase signals and

35                  - each successive multiplexer output leads its predecessor by a multiple of the predetermined time interval.

40                  20. A method of synthesizing an output signal with an output frequency higher than a reference frequency from a plurality of phase signals having the reference frequency with each phase signal being out of phase with adjacent phase signals by a multiple of a predetermined time interval, the method comprising:

45                  a) generating a select word from a stored value,

10 b) selecting a selected phase signal from the plurality of phase signals based on at least a portion of the select word,

c) generating an output signal from said selected phase signal,

15 d) repeating steps a) to c) for every cycle of the output signal.

21. A method as claimed in claim 20 further including the step of generating the plurality of phase signals.

22. A method as claimed in claim 20 wherein each successive output signal leads its predecessor by a multiple of the predetermined time interval.

C 23. A method as in claim 20 wherein step b) includes selecting at least two selected phase signals from the plurality of phase signals based on at least a portion of the select word.

24. A method as in claim 23 wherein step c) includes blending the at least two selected phase signals to produce the output signal.

25. A method as in claim 20 wherein step a) includes adding a predetermined control word to the stored value to produce a new stored value.